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3 μm Pitch, 1 μm Active Diameter SPAD Arrays in 130nm CMOS Imaging Technology

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Abstract— A shared well 4x4 SPAD array test structure with 3 μm pitch is realized in a 130nm CMOS image sensor technology. The SPADs have 150Hz median DCR at room temperature at 1V excess bias, 15% peak PDP and 176ps FWHM timing jitter both at 3V excess bias.

Index Terms— Single photon avalanche diode, photon counting, CMOS image sensor.

I. INTRODUCTION

CMOS Single Photon Avalanche Diode (SPAD) imaging arrays implemented with advanced CMOS process nodes, 3D-hybrid bonding and backside-illumination (BSI) offer a pathway towards digital photon counting cameras with high sensitivity, temporal resolution and dynamic range [1]. Such technologies solve the severe trade-off implicit in front-side illuminated (FSI) SPAD imagers between fill-factor and pixel functionality which are being addressed by analogue pixel techniques, shared-pixel layouts, microlenses and high temporal oversampling [2][3][4][5]. The advent of hybrid Cu-Cu direct bonding offers per-pixel connection between a dense SPAD-only top-tier with a photon counting, timing and readout matrix in the bottom-tier, decoupling the individual scaling challenges of detector, hybrid-bond and electronics towards small pixel pitches.

SPADs with active diameters as low as 2 μm have been investigated either as isolated test structures or in shared well arrays with source follower buffers at 5 μm pitch [6][7][8][9]. Recent reports of shared-well SPAD imagers at 7.83 μm and 8.25 μm pitch with fill-factors in excess of 50% point the way towards pixel pitches compatible with high-resolution imaging [1][10]. Apart from the loss of fill-factor, this scaling is attractive for many SPAD properties such as timing jitter, dark count rate and crosstalk which are improved as the detector volume and avalanche charge reduce [6]. A hybrid pixel combining Geiger-mode avalanche multiplication with a pinned-photodiode was recently proposed through modulation of a high voltage back-bias [11]. The 3.8 μm pitch 1Mpix BSI imager exhibits 100dB dynamic range and very low dark count. However, the avalanche mode operates without harnessing the photon counting and timing properties available from SPAD pixels.

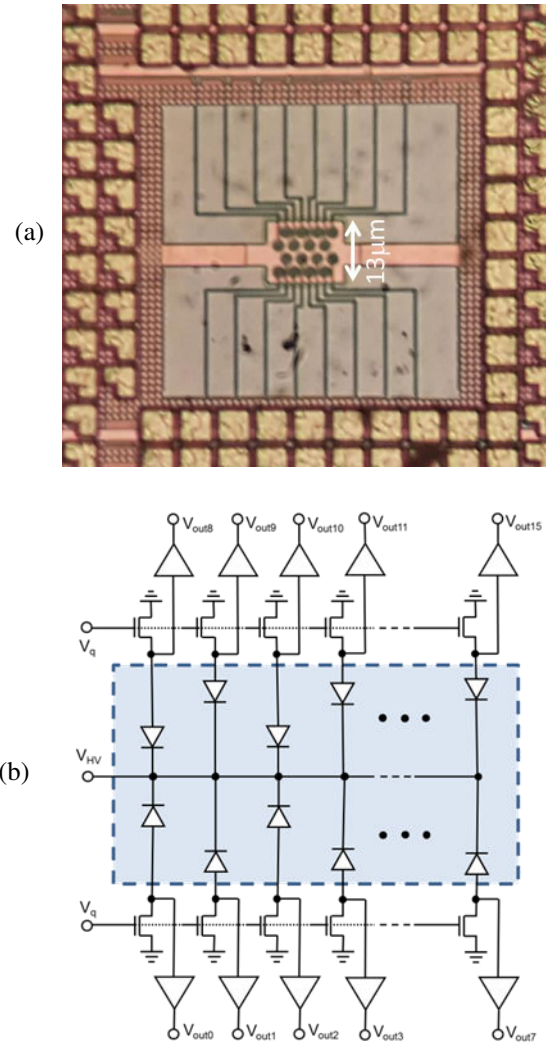


Fig. 1. 4 x 4 shared well SPAD array with individually accessible anodes (a) layout (b) circuit schematic.

In this paper we demonstrate the smallest pitch SPAD array in the literature suited to implementing future high resolution stacked SPAD imagers. Although the structure is implemented in a 130nm 4LM FSI CMOS image sensor technology, it could act as the top-tier BSI SPAD layer in a stacked imager by being inverted and ported to a BSI technology [1]. Section II describes the device structure, Section III the device measurements while Section IV discusses future perspectives for imaging arrays.

II. SPAD TEST STRUCTURE DESCRIPTION

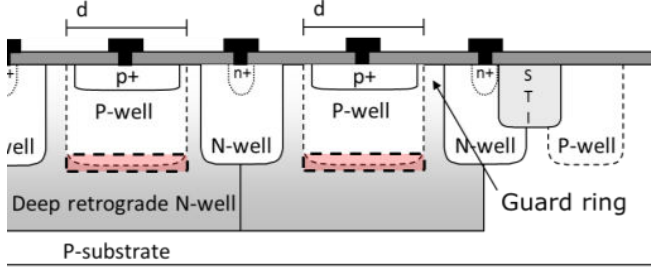


Fig. 2. Cross section through two SPADs sharing a common deep n-well cathode and the periphery of the array

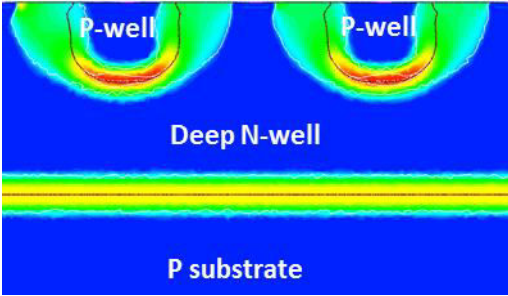


Fig. 3. TCAD electric field plot showing two multiplication regions (red) and low field guard rings (green)

The $3\ \mu\text{m}$ pitch 4×4 test structure (Fig. 1a) employs a scalable $1\ \mu\text{m}$ diameter SPAD structure [6]. The SPADs are arranged in a honeycomb style to maximize fill-factor achieving around 14%. All anodes of the 4×4 structure are wired individually to NMOS quench circuits and buffers placed a few microns away from the periphery of the shared well (Fig. 1b). A 16×16 silicon photomultiplier array of these devices has also been integrated and is the largest achievable without occluding the anodes with the 3 metal routing layers. Fig. 2 shows the device cross-section consisting of a p-well to retrograde deep n-well avalanche region and a virtual guard ring. Shared well arrays of this SPAD structure have been implemented at large pixel pitches and fill-factors in digital silicon photomultipliers [12], however never before at this extremely small dimension. TCAD simulation is used to confirm that the high field breakdown region is confined below the p-well and that a reduced field in the periphery acts as an effective guard ring (Fig. 3).

III. MEASUREMENT RESULTS

The breakdown voltage of the SPADs is 15.8V. A median dark count rate (DCR) of 150Hz is measured at 1V excess bias and room temperature. Fig. 4 shows a minimum dead time of 10ns limited by buffer drive strength and pad capacitive loading. Fig. 5 shows a 100k event inter-arrival time histogram of a SPAD biased at 1V excess bias operating with a dead time of 10ns. The region below 50ns shows an increase of pulse rate beyond the Poisson curve indicating an after-pulsing rate of 0.18%. Optical crosstalk is characterized by generating a histogram of the inter-arrival times (t_{diff}) of two devices revealing an uncorrelated noise floor and a sharp peak of a few 100ps FWHM around $t_{\text{diff}}=0$ (Fig. 6).

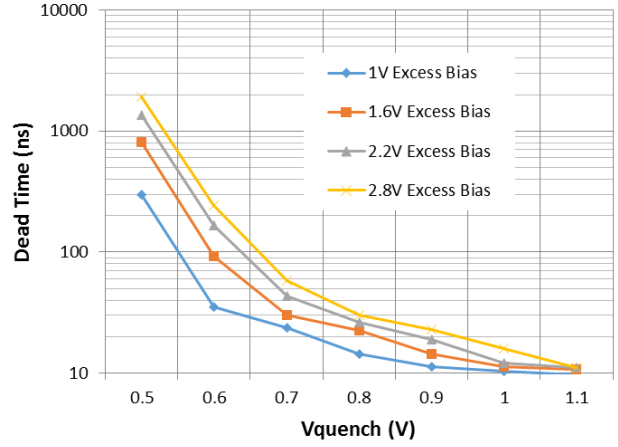


Fig. 4. SPAD dead time as a function of NMOS quench gate voltage.

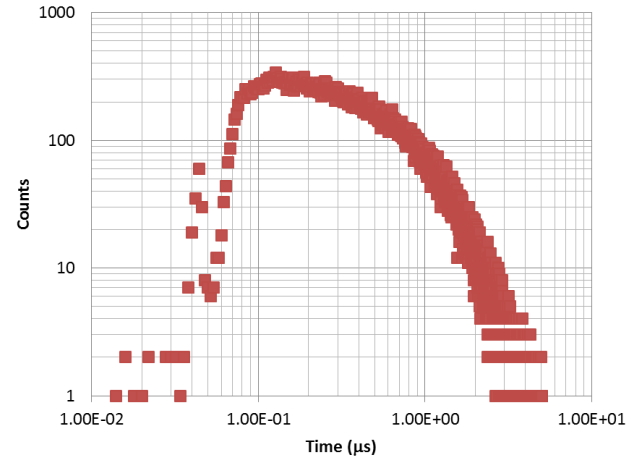


Fig. 5. Inter-arrival times of a SPAD operating at 1V excess bias and 10ns dead time.

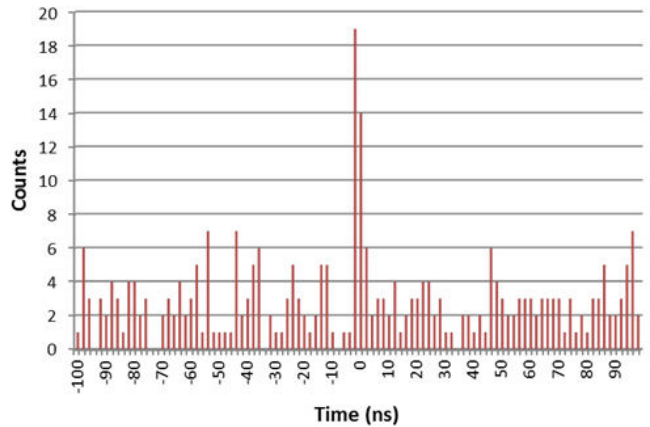


Fig. 6. Zoomed histogram of inter-arrival times of two different SPADs used to study optical crosstalk (15k events)

We count pulses in a region of $\pm 2\text{ns}$ around $t_{\text{diff}}=0\text{s}$ to perform our crosstalk calculation. This allows crosstalk to be studied in ambient conditions reducing acquisition times, and without the need to enable or disable device anodes [13].

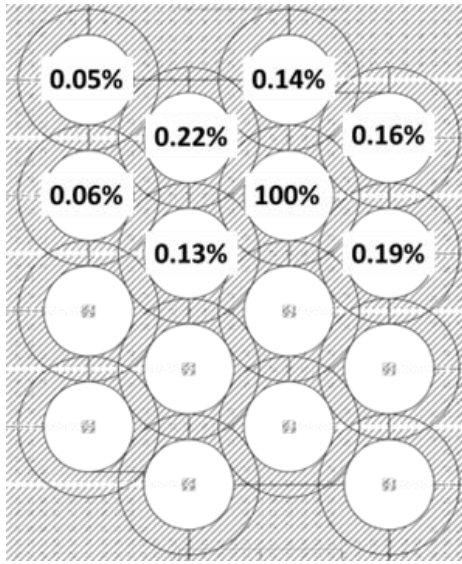


Fig. 7. Crosstalk map of the SPAD array at 1V excess bias.

Crosstalk is then calculated by integrating counts in the peak, compensated for the ambient count rate and dividing by the total number of events. As expected, the crosstalk is much lower (<0.2%) than larger devices and decreases with distance from the emitter (Fig. 7) [13].

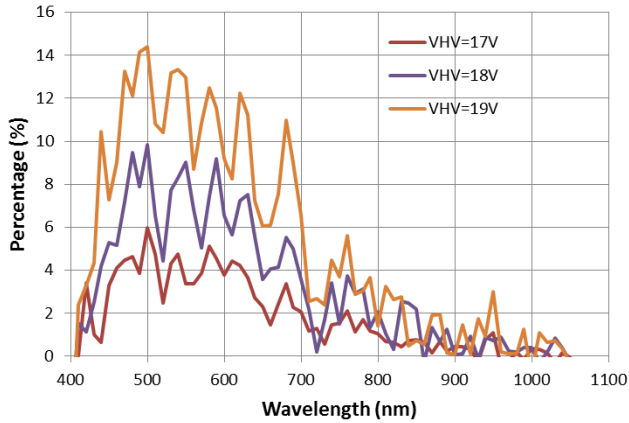


Fig. 8. Photon detection probability plotted against wavelength

Fig. 8 shows the spectral response of the detector. A peak photon detection (PDP) probability of 15% at 500nm is measured at 3.2V excess bias. This is a factor of 2-3x lower than larger diameter realizations of the same device structure [12][13]. The PDP increases linearly at 4%/V with excess bias and shows strong Fabry-Perot interference effects in the front-side 4 metal optical stack.

The SPAD timing jitter is plotted in Fig. 9 and Fig. 10. This was measured in response to two wavelengths of Hamamatsu PLP-10 pulsed lasers attenuated by neutral density filters to fraction of a photon per pulse. The timing jitter shows little voltage dependence and marginally higher full-width half maximum (FWHM) at the longer wavelengths. The jitter tail of these devices is short confirming the trend seen in previous measurements of such small devices [6].

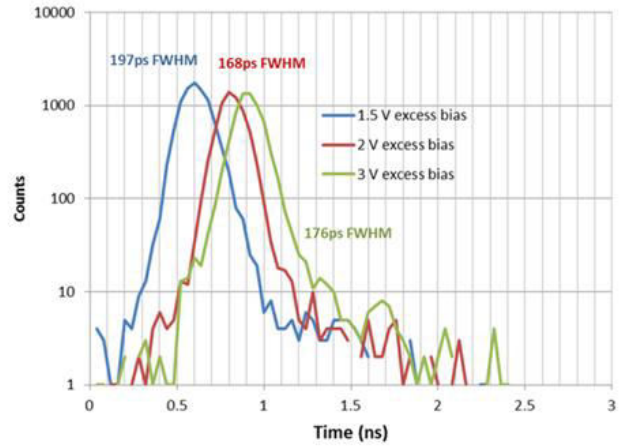


Fig. 9. Timing jitter of SPAD in response to a pulsed 445nm

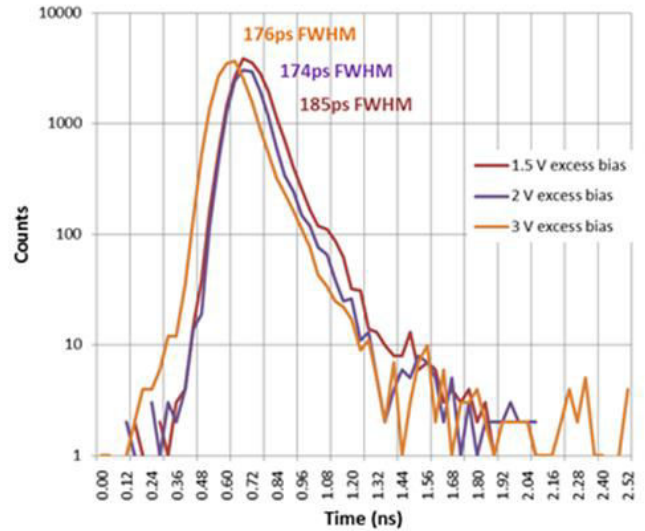


Fig. 10. Timing jitter of SPAD in response to pulsed 773nm laser

IV. DISCUSSION

The performance of the device is relatively poor compared to the state of the art (Table I). The device exhibits a high DCR per unit area (190Hz/ μm^2), an increased breakdown voltage, higher timing jitter and a lower PDP compared to larger devices of the same construction [6]. Although measurements of the variation of DCR with temperature and voltage indicate tunneling within the device, this behavior is not predicted by 2D TCAD simulation. More detailed modelling and investigation of the mechanism is being pursued.

Nevertheless, our test structure demonstrates that SPAD devices can be scaled to the small dimensions required for future high resolution quanta-image sensors (QIS). Few micron pitch SPAD arrays can then be employed in hybrid-bonded top tier pitch BSI imagers. This awaits progress in manufacturing of per-pixel hybrid bonds at such dimensions which is a topic of much industry activity. A key research question then arises; *how to realize photon counting and timing pixel electronic matrices in the bottom tier at these*

small pitches? Two approaches are immediately evident borrowing techniques proposed with limited fill-factor in front-side illuminated realizations. The first is the use of analogue pixels based on either gated photon counting or time to analogue conversion [14]. The second is the design of digital pixels in advanced nanometer process nodes to implement gated counters or time to digital converters [15].

V. CONCLUSION

A test structure demonstrates that SPAD devices can be scaled to the small dimensions required for future high resolution quanta-image sensors when ported to stacked BSI technologies. Further research into few micron pitch SPAD arrays is required to improve the device performance.

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	This Work	[6]	[7]	[9]	[11]
Technology	130nm CIS	130nm CIS	90nm CIS	90nm CIS	110nm BSI
Diameter (Pitch)	1 μ m (3 μ m)	2 μ m	2 μ m	2 μ m (5 μ m)	(3.8 μ m)
Junction/GR structure	p-well/p-epi	p-well/p-epi	p-well/p-epi	p-plus/n-well virtual	buried n-p
VBD @RT	15.8V	14.4V	17.7V	10.3V	23V
Median DCR/Area	190Hz/ μ m ² @1.2V	2.9Hz/ μ m ² @1.2V	0.39Hz/ μ m ² @1.2V	79.639Hz/ μ m ² @0.6V	0.88Hz/ μ m ² @2V
PDP Peak	15% @ 3.2V	14% @ 1.2V	33% @ 1.2V	36% @0.6V	-
Timing Jitter (FWHM)	185ps @ 3V	136ps @ 1.2V	103ps @ 1.2V	107ps @0.6V	-

Table I: Few micron diameter SPAD performance comparison