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Top-down convergence of near-infrared photonics with silicon substrate-integrated electronics

Martino Bernard,[1,*] Fabio Acerbi,[1] Giovanni Paternoster,[1] Gioele Piccoli,[1] Luca Gemma,[1,2] Davide Brunelli,[2] Alberto Gola,[1] Georg Pucker,[1] Lucio Pancheri,[2] and Mher Ghulinyan[1]

[1]Sensors and Devices, Fondazione Bruno Kessler, via Sommarive 18, 38123 - Trento, Italy
[2]Department of Industrial Engineering, University of Trento, via Sommarive 9, 38123 - Trento, Italy
*Corresponding author: bernard@fbk.eu

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On-chip direct coupling of dielectric waveguides to Si substrate-integrated photodetectors has been realized within a top-down approach. A first-run 44% external quantum efficiency at 850 nm is shown for an oxynitride photonic integrated circuit at room temperature.

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The full convergence of Si-based photonic integrated circuits (PIC) with CMOS electronics promises to pave the way toward mass-manufacturable, densely integrated, and cost-effective solutions. Silicon nitride (SiN) [1] and silicon oxynitride (SiON) [2] platforms, which are transparent at the visible and near-infrared (NIR) spectral regions, can benefit from homogeneous integration with Si photodetectors (PD) and readout electronics developed within the same substrate. Recent advances in *quantum* technologies have posed a further challenge to directly integrate single-photon avalanche diodes (SPADs) with quantum photonic architectures [3]. Several solutions have been reported: superconducting nanowire single-photon detectors [4] and transition edge sensors [5] offer extremely high photon detection efficiencies (PDEs) on the cost of operation at cryogenic temperatures. Ge-on-Si SPADs, coupled to Si waveguides with PDE ∼5.3% at 1310 nm and operating at 80 K were demonstrated [6].

Scalability and room-temperature operation could be straightforward to achieve in a top-down approach by integrating the PIC CMOS electronics in the Si substrate. First, the detectors (PDs, SPADs) and, potentially, all the control electronics are realized within the same substrate; second, the PIC is fabricated on top of it [7]. One major challenge of this approach is the requirement to isolate the photonic layer from the substrate within the light manipulation stage and to couple them at the detection point. PIC-to-detector coupling for NIR operation has been addressed in several works using evanescent Ge-on-Si [6] and SiN-on-SOI [8] or SOI grating-assisted approaches [9].

Here we demonstrate the direct integration of a SiON photonic circuit with photodetectors fabricated in the Si substrate within a single fabrication process. The optical waveguide-detector coupling is achieved by 3D structuring of the bottom cladding of the PIC through an efficient, CMOS-compatible process using a single lithography and wet-etching step [10]. The first devices show an external quantum efficiency (QE) of 44.3% at 850 nm wavelength with a large potential of improvement and a perspective of huge impact upon implementation to Si SPAD technology [11].

The photonic-electronic coupling is realized by shaping the bottom cladding of the PIC into a shallow-angled wedge form as shown in Fig. 1(a). The waveguides follow the cladding's profile and approach the substrate adiabatically at the PD locations where the optical mode leaks into the absorbing substrate. The light coupling efficiency from a SiON waveguide to the detector has been numerically simulated using the finite element method [Fig. 1(a)]. It considers (A) a stage of lossless propagation (full cladding height), (B) the region where the PIC follows a shallow descent toward the substrate, and (C) a portion of close proximity of the waveguide and the substrate, where the light refracts from the PIC into the Si epitaxial layer (*epi*-Si) at an angle $\theta_s \approx 26°$. This angle is given by the Snell's law as $\sin(\theta_s) = n_{\text{eff}}/n_s$, where $n_{\text{eff}} = 1.594$ and $n_s = 3.673$ are the mode refractive index in the waveguide and the refractive index of Si, respectively. Photons, absorbed in the *epi*-Si region, generate *e-h* pairs that are collected efficiently through the *p-n* junction. The amount of light absorbed within the *epi* layer depends on the *epi* layer thickness and the light wavelength. A coupling efficiency of 46% at a wavelength of 850 nm has been estimated from the fraction of the optical power absorbed within a 10 μm thick *epi*-layer and a 25 μm PIC-PD coupling length.

The devices were fabricated starting from *p*-doped epitaxial Si wafers. First, the detectors were realized in the 10 μm thick *epi*-layer by ion implantation of arsenic and boron for the n^+ and p^+ regions, respectively. The substrates were covered with a thin SiN layer, which acts as an etch-stop film during the definition of the 3D structured cladding. Then, a 1.5 μm thick SiO_2 film was deposited, in which wedge structures were realized at PD positions following patterning and wet-etching of the film. The SEM images in Figs. 1(b) and 1(c) show a highly smooth slope of 8°, which guarantees a low-loss and adiabatic approach of the waveguide to the substrate. The PIC layer is realized by depositing a 500 nm PECVD SiON film on top of the structured cladding, patterned and defined by reactive ion etching. Next, dopant activation at high temperature is followed by the deposition of a second thin SiN and

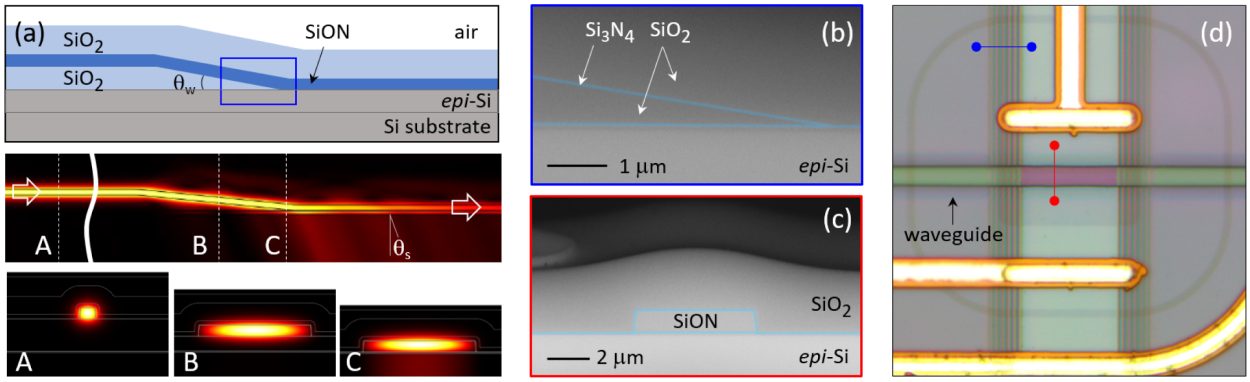

Fig. 1. (a) Sketch of the coupling method and numerical simulations. (A) Far from the detector, the 700 nm × 500 nm SiON waveguide travels on top of the 1.5 µm thick cladding without loss toward the substrate. (B) The waveguide width is adiabatically tapered to 5 µm before the descent toward the detector region. At the bottom of the wedge, the optical mode leaks into the Si substrate and is absorbed. Cross-sectional false-colored SEM images of the (b) 3D tapered cladding and (c) the waveguide on top of the PD. (d) An optical micrograph of the PIC-PD coupling region, with blue and red bars indicating the positions of shown SEM images.

a top cladding SiO_2. An Al-TiN stack is sputtered, patterned, and etched to allow for contacting the PDs (Al) and the thermo-optical control of the PIC (TiN).

The devices were first characterized by measuring the transmission of spiral waveguides of five different lengths to assess insertion and propagation losses, which at a wavelength of 850 nm result as 8.5 dB and 1.72 dB/cm, respectively. Second, light from a pig-tailed laser diode (Thorlabs LP850-SF80) was injected into the waveguides coupled to detectors, and the generated photocurrent was measured with a Kethley2450 sourcemeter. We estimated a total loss of 9.15 dB from fiber to the substrate-integrated detectors through 0.38 cm long waveguides [Fig. 2(a)]. The generated photocurrent was measured as a function of the applied voltage under different input laser intensities as shown in Fig. 2(b). The responsivity R of the detectors was calculated at a reference of −3 V bias [Fig. 2(c)] as the ratio of the photocurrent and the estimated optical power before the PIC-PD coupling region. The resulting $R \approx 0.3$ A/W corresponds to an external QE of 44.3%, which is very close to the simulated 46% of light power absorbed in Si. Furthermore, we envision that an optimization of the technology can significantly improve the PIC-detector coupling efficiency. This can be achieved by using up to 20 µm thick *epi*-layers, as well as by back-etching of the substrate, which induces a total internal reflection of unabsorbed photons back into the *epi*-layer. Preliminary simulations predict an improvement of the coupling efficiency up to 90% both for conventional Si PDs and SPAD devices operating at NIR wavelengths.

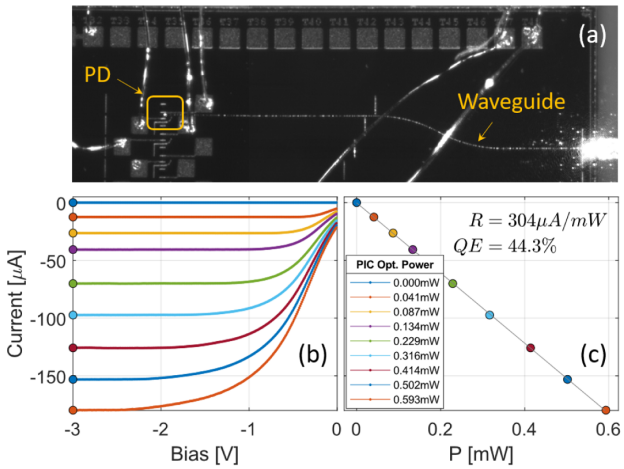

Fig. 2. (a) Optical image of the fabricated chip showing the trace of the waveguide and the PD region under operation. (b) The reverse bias IV-curves and (c) the photocurrent as a function of PIC optical power at −3 V bias.

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Disclosures. The authors declare no conflicts of interest.

Data Availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.

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