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Development of an open-source FEM simulation tool for aluminum PCBs based on PALACE-FEM

L. Baudino[a,b,c,*] **E. Botta**[a,b] **S. Beolé**[a,b] **D. Novel**[c,d] **A. Lega**[c,d] **and T. Facchinelli**[c,d]

[a] *Physics Department, University of Turin, Via Pietro Giuria, 1, 10125, Torino, TO, Italy*
[b] *INFN Turin, Via Pietro Giuria, 1, 10125, Torino, TO, Italy*
[c] *Fondazione Bruno Kessler, Via Sommarive, 18, 38123, Povo, TN, Italy*
[d] *INFN TIFPA, Via Sommarive, 14, 38123, Povo, TN, Italy*

E-mail: luca.baudino@unito.it

ABSTRACT: Aluminum PCBs are widely used in particle physics experiments because they offer a significantly lower material budget than traditional copper-based solutions (X_0: Al $\approx$ 8.9 cm, Cu $\approx$ 1.43 cm). This approach has already been adopted in several major experiments, such as ALICE ITS1/ITS2 and STAR. The integration of low material budget Kapton-aluminum PCBs with MAPS sensors is now being considered for next-generation detector systems, including IDEA (FCC-ee), ALICE3, and ePIC. Motivated by the growing interest within the community, Fondazione Bruno Kessler (FBK) started developing an innovative approach to Kapton-aluminum PCBs manufacturing. This effort has produced the first results, demonstrating its feasibility through the successful interconnection of an ALPIDE chip. The resulting PCB achieves an overall material budget of approximately 0.05%, comparable to the sensor X_0. To validate the electrical properties of these flexible PCBs, a dedicated simulation environment is required. For this reason, the goal of this work is to develop a comprehensive simulation tool capable of incorporating realistic PCB properties derived from material-characterization techniques such as resistivity analysis or precise cross-section measurements with Plasma Focused Ion Beam (PFIB). This work focuses on Geant4 simulations and on Finite Element Method (FEM) simulations performed using the open-source Palace framework to model the flexible PCB structures with high precision. In the initial phase, different mesh sizes and refinement parameters were varied to identify the optimal trade-off between computational cost and solution accuracy, with simulation results validated against IPC-2251 standards.

KEYWORDS: Detector design and construction technologies and materials; Detector modelling and simulations I (interaction of radiation with matter, interaction of photons with matter, interaction of hadrons with matter, etc); Particle tracking detectors; Special cables

*Corresponding author.

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1 Low material budget readout electronics for high-energy physics experiments

Silicon detectors represent the state-of-the-art technology for many particle physics measurements, owing to their excellent spatial and timing resolution. In particular, Monolithic Active Pixel Sensors (MAPS) have been widely adopted in High-Energy Physics experiments, as they are fabricated using commercial CMOS processes, which makes them cost-effective and suitable for large-area detector systems. Recent advances in CMOS technology have enabled progressively smaller feature sizes, leading to detectors with increasingly finer pixel pitches. Notable examples include the 180 nm technology employed in the ALICE ITS2 [1] and the 65 nm node foreseen for the ALICE ITS3 upgrade [2]. While higher detector granularity translates into improved spatial resolution, it also implies a larger number of channels and higher power consumption, demanding more extensive readout electronics and consequently increasing the material budget of the transmission lines. Since the thickness of silicon sensors cannot be easily reduced, typically ranging between 50 and 100 µm, minimizing the material budget of the associated electronics becomes a critical challenge.

In this context, Fondazione Bruno Kessler (FBK) is developing Kapton-aluminum flexible PCBs as an alternative to conventional copper-based transmission lines. The use of aluminum is motivated by its significantly larger radiation length ($X_0 \approx 8.9$ cm) compared to that of copper ($X_0 \approx 1.43$ cm), enabling a substantial reduction of the overall material budget.

Building upon the work presented in [3], we are developing a simulation framework to study the electrical behavior of Kapton-aluminum interconnects. In this work, we present the first simulation results for an FBK flexible PCB prototype, with a focus on material budget, insertion loss, and return loss. The reliability of the simulations is assessed through comparisons with Vector Network Analyzer (VNA) measurements and predictions based on IPC-2251 standards [4].

2 Preliminary Geant4 simulations

To evaluate the material budget of the proposed design, we developed a simulation interface based on Geant4 [5]. Geant4 version 11.3.2 was used with the QBBC physics list, which is recommended for accurate simulation of low-energy proton transport in the energy range below 1 GeV.[1] The interface is

[1] https://geant4.web.cern.ch/documentation/dev/plg_html/PhysicsListGuide/reference_PL/QBBC.html.

fully configurable through a dedicated configuration file and requires as input only the device geometry, provided as a GDML file, enabling fast simulations and straightforward comparisons between different detector geometries. This interface allows the extraction of two-dimensional material budget maps with a spatial resolution of $50 \times 50\,\mu\text{m}^2$ (figure 1). In addition, it provides detailed information on particle interactions and shower development within the structure for different types of incident particles.

Using this framework, we simulated the full stack design presented in [3]. The structure consists of two Kapton-aluminum layers, with Kapton and aluminum thicknesses of 25 µm and 20 µm respectively, an epoxy adhesive layer, a 50 µm-thick ALPIDE chip, and a final Kapton-aluminum bonding layer. The simulation yields a material budget of $X/X_0 \approx 0.1\%$ in the most densely populated region of the stack, corresponding to the ALPIDE pad area shown in figure 1, while an average value of approximately 0.05% is obtained across the remaining regions of the device. The material budget can be estimated either by simulating showers of charged particles (in this case 200 MeV protons or 10 MeV electrons) and measuring the deposited energy and scattering angle for each layer, or by using geantino beams as done in [6]. The latter method does not provide physical observables beyond the material budget itself, but is faster and computationally less demanding.

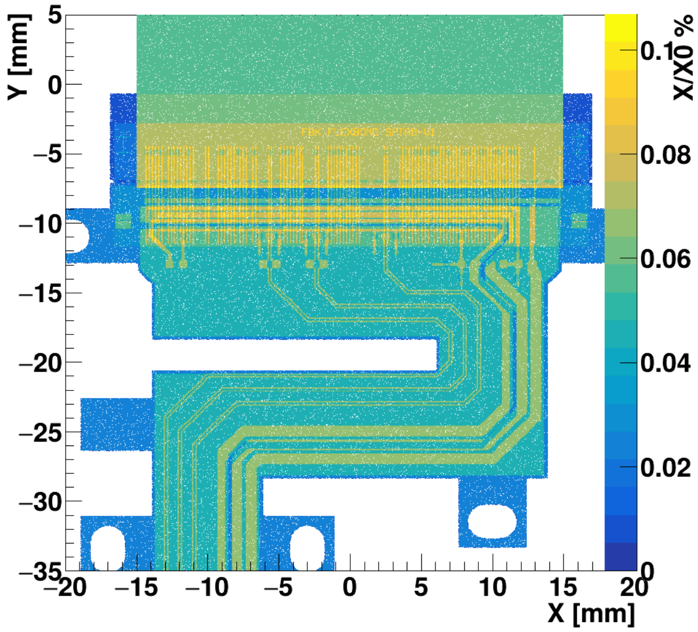

Figure 1. X/X_0 map of a multilayer Kapton-aluminum stack including an ALPIDE chip.

A comparison with a similar Kapton-copper stack reported in [7], where a material budget of $X/X_0 = 0.1\%$ was achieved excluding the copper layer, suggests that the proposed Kapton-aluminum flexible interconnect can achieve a substantially lower overall material budget.

3 FEM-simulation of extended flexible PCB layouts

A comprehensive analysis based on Finite Element Method simulations enables the extraction of key parameters such as the S-matrix, crosstalk, and electric and magnetic field distributions, as well as accurate computation of conductor and dielectric losses, including skin-effect contributions at high

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frequency. For this purpose, we selected Palace,[2] an open-source FEM framework that requires only geometry files as input, making it possible to integrate it with the Geant4 interface described above into a unified simulation pipeline. Palace was further chosen for its high degree of customization in mesh generation, port definitions, and boundary conditions.

While the final goal is to model the full design presented in [3], this work focuses on simple Coplanar Waveguide (CPW) structures, with results validated against IPC-2251 standards [4] and VNA measurements. A centimeter-scale line with a trace width of 90 µm was considered at different mesh sizes. To assess the agreement of our simulations over the 0.05–2 GHz frequency range with theoretical predictions (red line in figure 2), dispersion bands of 2%, 3%, and 4% around the expected value were considered. A χ^2 test with 20 degrees of freedom was then performed on the simulation with the lowest mesh size for each of the three hypotheses, yielding $\chi^2_{2\%} = 42.24$, $\chi^2_{3\%} = 18.77$ and $\chi^2_{4\%} = 10.56$. These results show that a 3% dispersion band best reproduces the average deviation of the simulated data from the theoretical value within the selected frequency range.

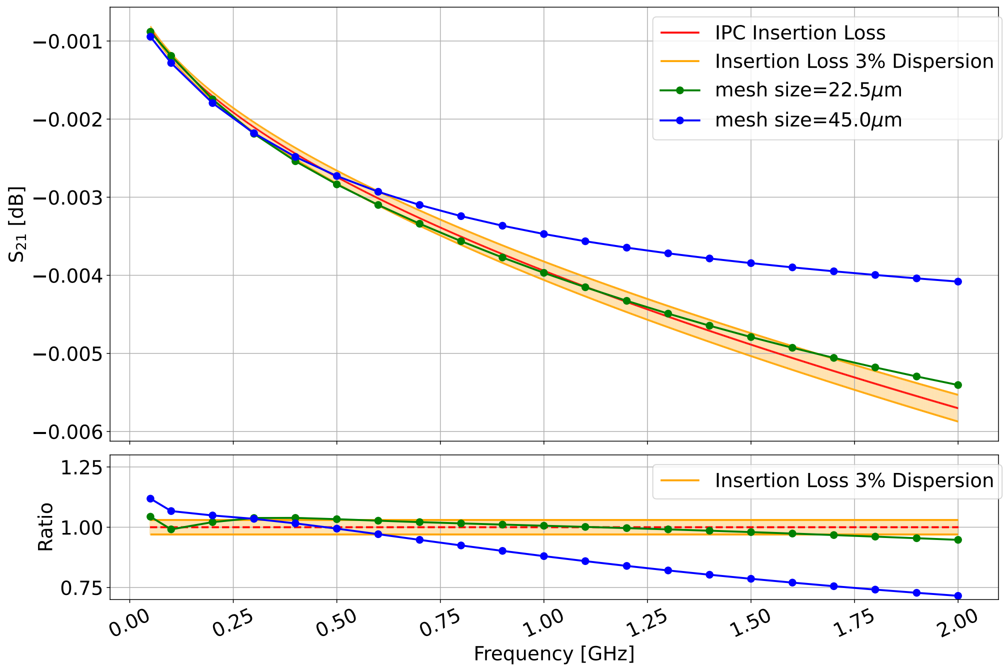

Figure 2. Simulated insertion loss (S_{21}) for a 1 cm Kapton-aluminum finite-ground CPW line with 90 µm trace width and 100 µm gap spacing, compared against the IPC-2251 analytical prediction and its 3% tolerance band. The finer mesh (22.5 µm) remains within the tolerance band across the full 0.05–2 GHz range, while the coarser mesh (45 µm) exhibits increasing deviation at higher frequencies. The ratio panel confirms that accurate results require a mesh size comparable to or smaller than the characteristic dimensions of the CPW geometry.

Electric and magnetic field distributions are also available from the simulation, enabling the evaluation of radiated power losses from the CPW. The simulated electric and magnetic fields were subsequently fitted using a conformal mapping model [8] and the Biot-Savart law, respectively, to extract the voltage and current at the CPW supply port. The extracted values of 7 ± 1 V and 0.13 ±

[2] https://awslabs.github.io/palace/stable/.

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0.01 A are in good agreement with the lumped port reference values of 7.07 V and 0.14 A, confirming the correct configuration of the simulation setup.

4 Radiation effects in open-ended structures

The simulation workflow was optimized to accurately predict conductor and dielectric power losses in the transmission line. However, Palace proves largely insensitive to radiation losses when the circuit operates as a millimeter-scale antenna in an open-ended configuration. To investigate this effect, we simulated open-ended structures of various lengths and introduced a data-driven scaling factor, defined as the ratio between the simulated and VNA-measured return loss. The scaling factor ranges from 0.01 for a line length of 200 µm up to 0.4 for a length of 5200 µm, approaching unity for a 1 cm CPW.

To demonstrate that agreement between simulations and the expected return loss improves further as the open-ended line exceeds centimeter-scale lengths, we simulated a 2 cm open-ended line over the frequency range 0–50 GHz. The expected S_{11} resonance pattern was successfully reproduced: the largest resonance peak was found at 8 GHz, corresponding to a propagating wave with $\lambda \approx 2$ cm, while the spacing between consecutive peaks was approximately 3.5 GHz, in good agreement with the value predicted by equation (4.1):

$$\Delta f = \frac{1}{\Delta t} = \frac{c}{2\sqrt{\varepsilon_{\text{eff}}}L} \tag{4.1}$$

where $L = 2$ cm is the line length, c is the speed of light in vacuum, and $\varepsilon_{\text{eff}} = 4.8$ is the effective dielectric constant of the simulated CPW.

5 Conclusions

The objective of this work was to develop a comprehensive simulation framework for the efficient evaluation of Kapton-aluminum flexible PCB prototypes and to gain insight into their performance prior to fabrication. The integration of electrical simulations with Geant4 analysis provides a powerful tool for better understanding the trade-off between minimizing the material budget, reducing particle interactions, and optimizing signal integrity.

The material budget results presented in section 2 show a significantly lower value compared to those of analogous Kapton-copper circuits [7]. This improvement could enable, in future developments, the extension of Kapton foils to fully encapsulate the silicon chip, resulting in a more modular and robust device, with the potential to simplify the assembly of large-area detector systems.

The next phase of the project will focus on the realization of a new flexible cable connected to an ALPIDE chip, building upon the work presented in [3]. The new prototype will be designed and optimized according to stringent high-frequency design rules, and its performance will be validated at 1.2 Gbps, the maximum readout speed of the chip, using a dedicated FPGA-based readout system and through further VNA characterization.

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